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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/537,274	03/29/2000	Larry Eugene Mosley	884.240US1	7167

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EXAMINER	
THOMAS, ERIC W	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 04/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/537,274	Applicant(s) MOSLEY, LARRY EUGENE	
	Examiner Eric W Thomas	Art Unit 2831	

-- The MAILING DATE of this communicati n appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-10, 14-18* is/are allowed.

6)☒ Claim(s) *1-5,8,11,13,19 and 21* is/are rejected.

7)☒ Claim(s) *6,7,12 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsp rson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/8/02 has been entered.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

Claim 1, line 11, change "conductor" to –conductive--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5, 8, 11, 13, 19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herrell et al. (US 6,191,479) in view of Naito et al. (EP 0917165) .

Herrell et al. disclose in fig. 1 a multi layer integrated circuit capacitor comprising: a substrate (12); a first conductive layer (13) located over and contacting the substrate;

a first insulator layer (18) located over and contacting the first conductive layer, the first insulator layer not contacting the substrate; a second conductive layer (14) located over the first insulator layer; a second insulator layer (24) located over the second conductive layer; a plurality of conductive vias (fig. 4A-5B) downwardly extending through the top (second) insulator layer to provide electrical interconnection to the first and second conductive layers

Herrell et al. do not disclose a third conductive layer located over the second insulator layer; and a third insulator layer located over the third conductor layer; wherein the plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the third conductor layer. It should be noted that Herrell et al. disclose that the number of conductive layers is not limited.

Naito et al. teach (fig. 1) the use of a third conductive layer located over a second insulator layer; and a third insulator layer located over the third conductor layer; wherein a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductor layers.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to add a third conductive layer and a third insulator layer to the capacitor of Herrell et al., since such a modification would improve the capacitance of the system.

Regarding claim 2, Herrell et al. disclose C4 lands (col. 6 lines 14-40) are formed on the upper insulator layer.

Regarding claim 3, Herrell et al. disclose (see fig. 1, 4A-5B) that the C4 lands are fabricated in staggered columns in a plan view.

Regarding claim 4, the modified Herrell et al. disclose the electrode can be formed of a metal material and the insulator layers are formed from barium strontium titanate (see col. 10 lines 5-30).

Regarding claim 5, the modified Herrell et al. disclose the claimed invention except for at least one of the conductive layer is formed from a copper material. Copper electrodes (conductive layer) are well known in the capacitor art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductive layers of Herrell et al from a copper material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 8, the modified Herrell et al. disclose plurality of conductive vias pass through the second conductive layer without forming an electrical connection with the second conductive layer.

Regarding claim 11, the modified Herrell et al. disclose (as seen above) a circuit capacitor comprising a substrate; a first conductive layer located over and contacting the substrate; a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate; a second conductive layer located over the first insulator layer; a second insulator layer located over the second conductive layer; a third conductive layer located over the second insulator layer; a third

insulator layer located over the third conductive layer; a first plurality (see fig. 4A-5B) of conductive vias downwardly extending through the third insulator layer, the third conductive layer, the second insulator layer, the second conductive layer and the first insulator layer to provide electrical interconnection to the first and third conductive layers; and a second plurality (see fig. 4A-5B) of conductive vias downwardly extending through the third insulator layer, the third conductive layer, and the second insulator layer to provide electrical interconnection to the second conductive layer.

Regarding claim 13, the modified Herrell et al. disclose the electrode can be formed of a metal material and the insulator layers are formed from barium strontium titanate (see col. 10 lines 5-30).

Regarding claim 19, the modified Herrell et al. disclose (as seen above) a multi layer integrated circuit capacitor comprising: a substrate; a first conductive layer located over and contacting the substrate; a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate; a second conductive layer located over the first insulator layer; a second insulator layer located over the second conductive layer; a third conductive layer located over the second insulator layer; a third insulator layer located over then third conductive layer; and a plurality of conductive vias downwardly extending thought the third insulator layer to provide electrical interconnection to the first, second, and third conductive layers, the plurality of conductive vias further extends through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the integrated circuit capacitor.

Regarding claim 21, the modified Herrell et al. disclose the electrode can be formed of a metal material and the insulator layers are formed from barium strontium titanate (see col. 10 lines 5-30).

Allowable Subject Matter

5. Claims 9-10, 14-18 are allowed.

6. Claims 6-7, 12, 20 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or fairly suggest (taken in combination with the other claimed features) a multilayer circuit capacitor comprising a fourth conductive layer located overt the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias (claims 6, 12, 20); the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer (claim 7); a first conductive layer located over and contacting the first conductive layer the insulator layer not contacting the substrate, a second conductive layer located over the first insulator layer being fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer (claims 9-10); a second integrated circuit die mounted on the circuit board and electrically connected to

the supply voltage interconnect lines, the second integrated circuit die comprising a capacitor having a first insulator layer located over and contacting the first conductive layer the first insulator layer not contacting the substrate (claims 14-18).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is (703) 305-0878. The examiner can normally be reached on Mon & Sat 9:00 AM - 9:30 PM;Tue-Fri 5:30PM-10:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 703-308-3682. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

ewt
April 17, 2002

Dean A. Reichard 4/19/02

DEAN A. REICHARD
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